1. A redundancy structure for implementation of redundant circuits within an integrated circuit placed on a semiconductor substrate including a fusible link whereby said fusible link comprises:

a layer of a conductive material deposited upon an insulating layer of said semiconductor substrate connected between the redundant circuits and other circuits present on said integrated circuit;

a hard mask layer placed upon said layer of conductive material during transistor processing to protect said layer of conductive material and removed from said layer of conductive layer before deposition of interlayer dielectric layers on said semiconductor substrate to improve a fuse destruction to implement said redundant circuits;

an opening in said interlayer dielectric layers to thin said interlayer dielectric layers to allow exposure of said layer of conductive material to facilitate destruction of said layer of conductive material.

2. The redundancy structure of claim 1 wherein said layer of conductive material is selected from a group of conductive materials consisting of metals, heavily doped polycrystalline silicon, and alloys of metals and heavily doped polycrystalline silicon.

3. The redundancy structure of claim 1 wherein the insulating layer is a field oxide.

4. The redundancy structure of claim 1 wherein the redundant circuit is a column of a DRAM array.

5. The redundancy structure of claim 1 wherein the redundant circuit is a row of a DRAM array.

6. The redundancy structure of claim 1 wherein the hard mask layer is silicon nitride.

7. The redundancy structure of claim 6 wherein a thickness of the silicon nitride of said hard mask layer is from approximately 1500Å to approximately 3000Å.

8. The redundancy structure of claim 1 wherein the hard mask layer is comprised of two layers, whereby a first layer is silicon dioxide and a second layer is silicon nitride.

9. The redundancy structure of claim 8 wherein the first layer of silicon dioxide has a thickness of from approximately 100Å to approximately

1000Å and the second layer of silicon nitride has a thickness of from approximately 1000Å to approximately 3000Å.

10. The redundancy structure of claim 1 wherein the opening has a bottom portion of said opening in said interlayer dielectric extends to between 4000Å and approximately 10,000Å of said layer of conductive material.

11. The redundancy structure of claim 1 wherein the interlayer dielectric is an undoped oxide and a borophososilicate glass.

12. The redundancy structure of claim 1 wherein the interlayer dielectric at a bottom portion of the opening in the interlayer dielectric has sufficient transparency to allow destruction of the layer of conductive material.

13. The redundancy structure of claim 1 wherein the removed hard mask layer is too thick to allow destruction of said layer of conductive material.

14. A method of forming a fusing structure to implement redundancy circuits within integrated circuit on a semiconductor substrate comprising the steps of:

forming at least one fuse link of a conductive material on an insulating layer on said semiconductor substrate simultaneously with formation of gate layers of transistors within said integrated circuits;

forming a hard mask layer on said fuse links simultaneously with the formation of a hard mask layer on said gate layers;

forming sources and drains of the transistors of the integrated circuits; and

placing a hard mask removal resist material on the surface of the semiconductor substrate having openings at said fuse links and said gate layer; and

removing said hard mask on said fuse link simultaneously with said gate layer.

15. The method of claim 14 further comprising:

forming interlayer dielectric on the surface of the semiconductor substrate; and

forming self-aligned contacts to the sources and drains of the integrated circuits; and

simultaneously forming an opening above the fuse links.

16. The method of claim 14 wherein the fuse links are formed of a group of conductive materials consisting of metals, heavily doped polycrystalline silicon, and alloys of metals and heavily doped polycrystalline silicon.

17. The method of claim 14 wherein said insulating layer onto which said fuse links are formed is a field oxide.

18. The method of claim 14 wherein said redundant circuit is a column of a DRAM array.

19. The method of claim 14 wherein said redundant circuit is a row of a DRAM array.

20. The method of claim 14 wherein said hard mask layer is formed of a silicon nitride.

21. The method of claim 20 wherein said hard mask is formed to a thickness of from approximately 1500Å to approximately 3000Å.

22. The method of claim 14 wherein the hard mask layer is formed of two layers, whereby a first layer is silicon dioxide and a second layer is silicon nitride.

23. The method of claim 22 wherein the first layer is formed to a thickness of from approximately 100Å to approximately 1000Å and the second layer is formed to a thickness of from approximately 1000Å to approximately 3000Å.

24. The method of claim 15 wherein said opening is formed until a bottom portion of said opening extends to within 4000Å and approximately 10,000Å of said layer of conductive material.

25. The method of claim 15 wherein said interlayer dielectric is formed of an undoped oxide and a borophososilicate glass.

26. The method of claim 15 wherein the opening in the interlayer dielectric is formed such that said interlayer dielectric between a bottom portion of said opening and said fuse links are sufficiently transparent to allow destruction of said fuse links.

27. The method of claim 14 wherein said hard mask on said fuse links is formed to a thickness too great to allow reliable destruction of said fuse links.

28. An integrated circuit formed on a semiconductor substrate comprising:

A redundant circuit function having at least one fuse link structure to implement said redundant circuit function within said integrated circuit, whereby said fuse link structure is comprising:

a layer of a conductive material deposited upon an insulating layer of said semiconductor substrate

connected between the redundant circuits and other circuits present on said integrated circuit;

a hard mask layer placed upon said layer of conductive material during transistor processing to protect said layer of conductive material and removed from said layer of conductive layer for deposition of interlayer dielectric layers on said semiconductor substrate to improve a fuse destruction to implement said redundant circuits; and

an opening in said interlayer dielectric layers to thin said interlayer dielectric layers to allow exposure of said layer of conductive material to facilitate destruction of said layer of conductive material.

29. The integrated circuit of claim 28 wherein said layer of conductive material is selected from a group of conductive materials consisting of metals, heavily doped polycrystalline silicon, and alloys of metals and heavily doped polycrystalline silicon.

30. The integrated circuit of claim 28 wherein the insulating layer is a field oxide.

31. The integrated circuit of claim 28 wherein the redundant circuit is a column of a DRAM array.

32. The integrated circuit of claim 28 wherein the redundant circuit is a row of a DRAM array.

33. The integrated circuit of claim 28 wherein the hard mask layer is silicon nitride.

34. The integrated circuit of claim 28 wherein a thickness of the silicon nitride of said hard mask layer is from approximately 1500Å to approximately 3000Å.

35. The integrated circuit of claim 28 wherein the hard mask layer is comprised of two layers whereby a first layer is silicon dioxide and a second layer is silicon nitride.

36. The integrated circuit of claim 28 wherein the first layer of silicon dioxide has a thickness of from approximately 100Å to approximately 1000Å and the second layer of silicon nitride has a thickness of from approximately 1000Å to approximately 3000Å.

37. The integrated circuit of claim 28 wherein the opening has a bottom portion of said opening in said interlayer dielectric extends to between 4000Å and approximately 10,000Å of said layer of conductive material.

38. The integrated circuit of claim 28 wherein the interlayer dielectric is an undoped oxide and a borophososilicate glass.

39. The integrated circuit of claim 28 wherein the interlayer dielectric at a bottom portion of the opening in the interlayer dielectric has sufficient transparency to allow destruction of the layer of conductive material.

40. The integrated circuit of claim 28 wherein the removed hard mask layer is too thick to allow destruction of said layer of conductive material.